Background: Long Timing Effects

Jakob Engblom

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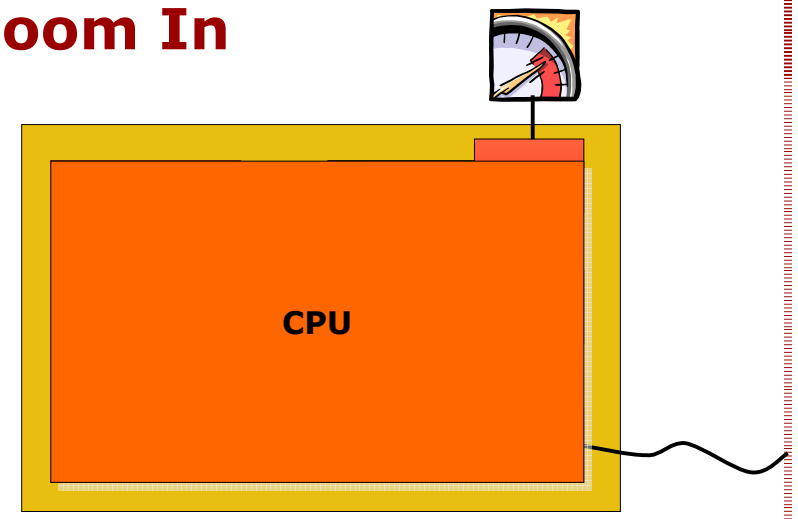
Zoom In



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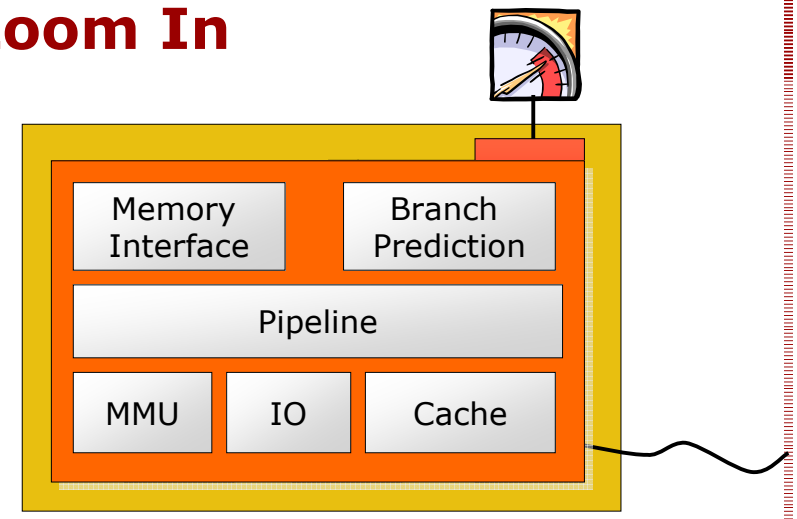
Zoom In



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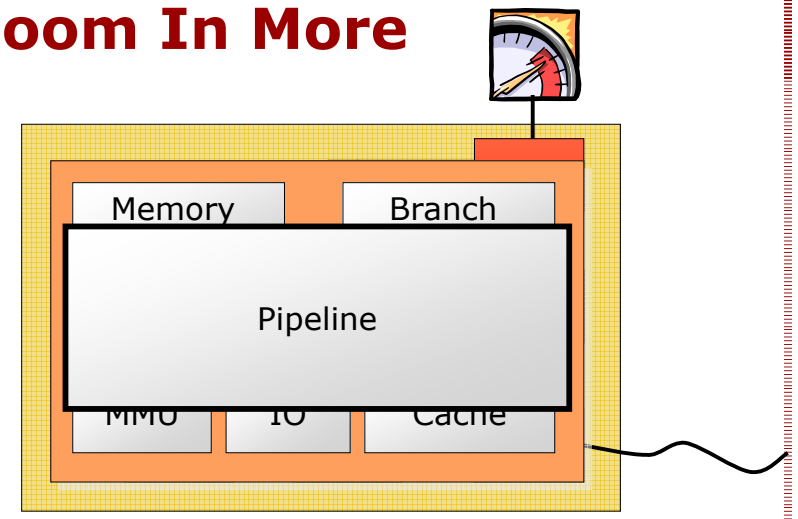
Zoom In More



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Long Timing Effects

- Unfortunately, it will be a "what did I do" talk.
- Concept from my PhD thesis
- Captures something essential

Background

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Program Timing Model

- Times (t_A)
  - For single nodes
- Timing effects (δ_{ABC})
  - For sequences of nodes
  - Pairwise or long (>2 nodes)
  - Effect of differing initial conditions
- Execution time: $T(A..Z)=\Sigma\ t + \Sigma\ \delta$
  - All times & all subsequences for A..Z

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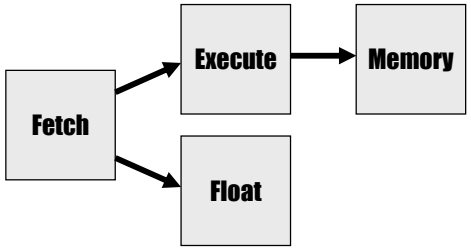
Program Timing Model

- Deriving timing effects:
  - For sequence
  - $\delta_{A..Z}=T(AB..YZ)-T(AB..Y)-T(B..YZ)+T(B..Y)$
  - Negative for speedup
  - Positive for slowdown
  - $\delta_{AB}=T(AB)-T(A)-T(B)$: Pairwise effects
- $\delta_{A..Z}\neq 0$ means that A affects Z

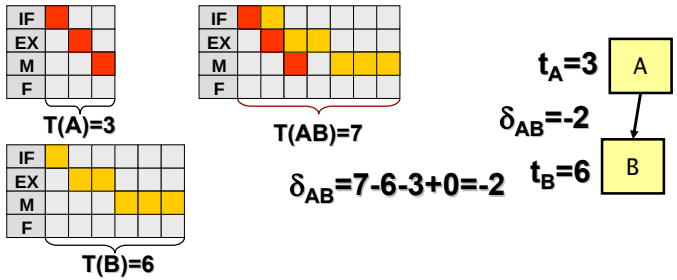
Example Pipeline Model

- Used in all examples ahead



Pairwise Timing Effects

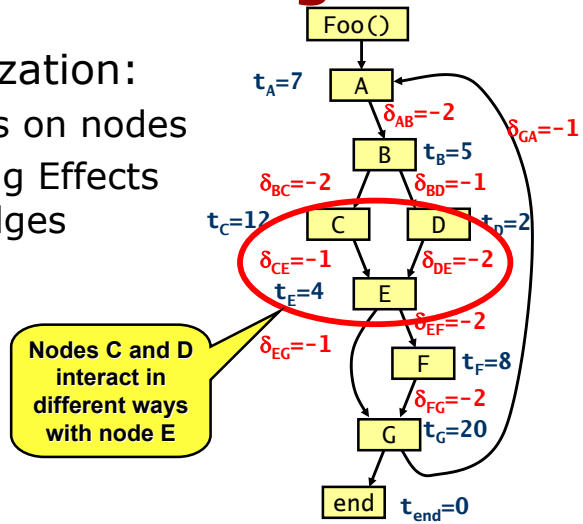
- Effects between two instr:



- "Always" appear in pipelines
- Always negative or zero

Pairwise Timing Effects

- Visualization:
  - Times on nodes
  - Timing Effects on edges



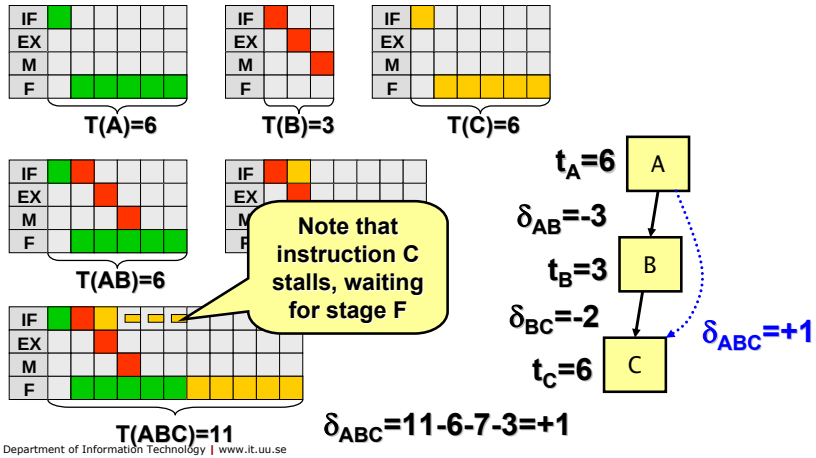
Long Timing Effects

Long Timing Effects

- TE across more than two blocks
- Property of the pipeline, not of our particular model
- Negative ($\delta_{A..Z} < 0$):
  - Can be safely ignored
- Positive ($\delta_{A..Z} > 0$):
  - Have to be considered for safety
  - The main problem in pipeline modeling for static WCET analysis

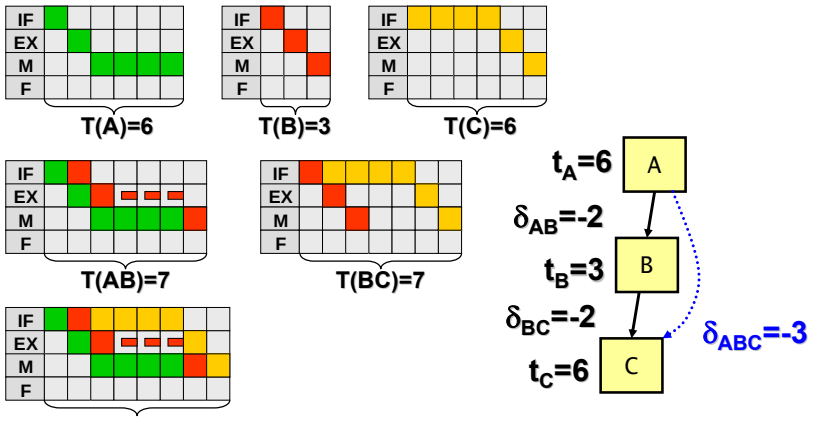
Long Timing Effect (LTE)

- In a parallel pipeline



Long Timing Effect (LTE)

- In a single in-order pipeline

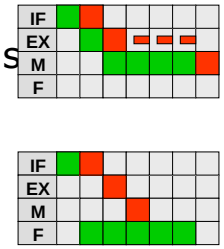


Consequences of LTEs

- Timing analysis
  - Has to consider more interactions
  - Higher complexity of analysis
  - Higher computational cost
- Programmer understandability
  - Harder to understand program timing
- Avoid = great simplification

Source of LTEs

- We have proven that LTEs over I_1 .. I_m require that:
  - The first instruction (I_1) stalls one of its successors
    OR
  - The first instruction (I_1) reaches past I_2 .. I_{m-1}
- NB: not sufficient condition



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Source of LTEs

- One stall can give several LTEs
- A single stall can give
  - Positive, and
  - Negative timing effects
- A stall need not give LTEs
  - Depends on exact timing of instructions
  - Many such cases on the V850E

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Only Negative LTE

- Prove absence of positive δ
- Only negative LTEs requires:
  - Single pipeline
  - All data dependences go between adjacent instructions
- Multiple pipelines means +
- Non-adjacent data dep means +

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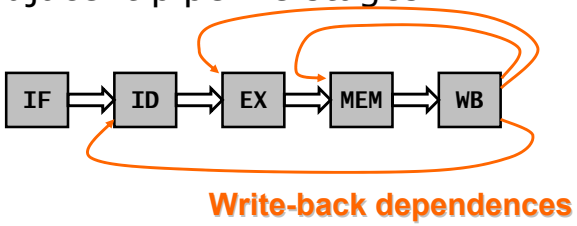
Only Negative LTEs

- Some lucky processors have no LTEs
- Examples:
  - NEC V850
  - ARM7, ARM9
  - Most five-stage RISC pipelines
- Allows safe approximate analysis
  - Analyze sequences up to some length /
  - Can be very tight & efficient
- Simple = analyzable

Only Negative LTE

- Data dependence between adjacent instructions only:
  - Data forwarding (not wait for WB)
  - Dependence only between adjacent pipeline stages



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Only Negative LTE

- Data dependence between adjacent instructions only:
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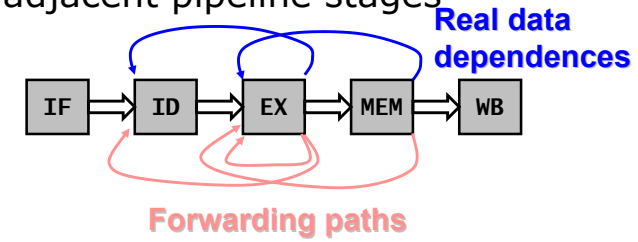

Unbounded LTEs

Unwanted guests

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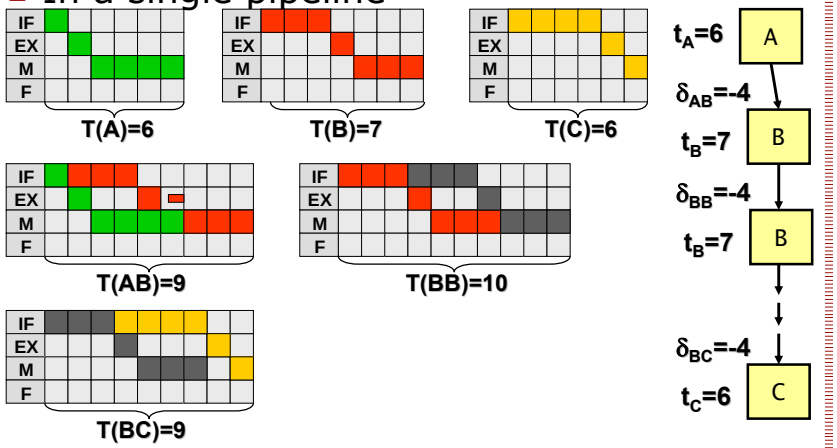
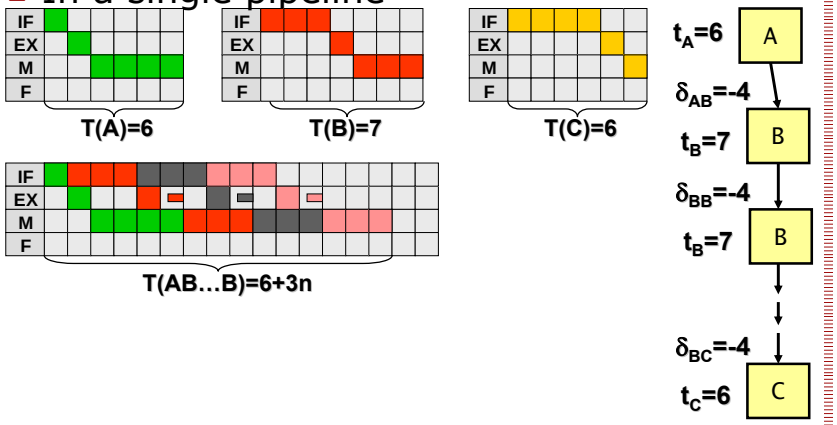
Unbounded LTE

- In a single pipeline



Unbounded LTE

- In a single pipeline



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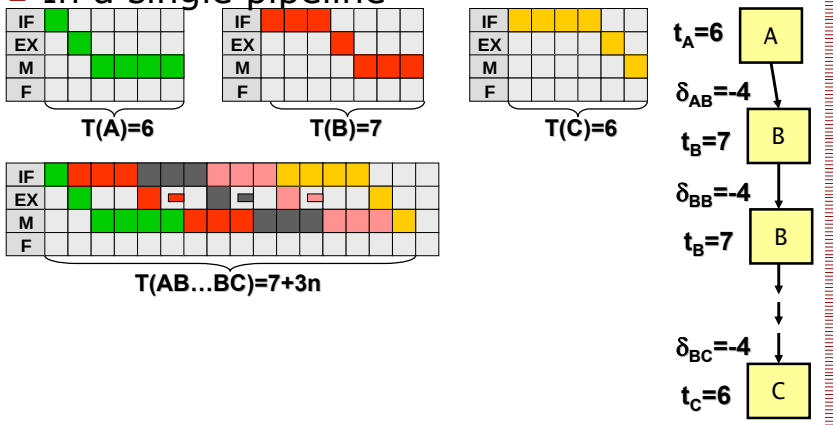
Unbounded LTE

- In a single pipeline



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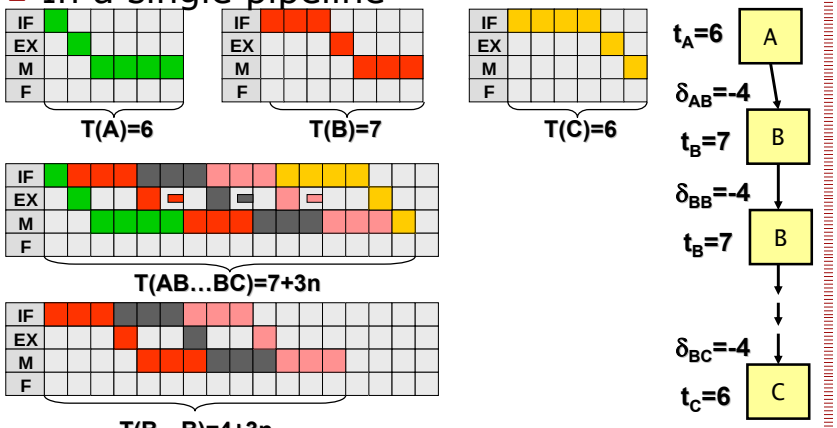
Unbounded LTE

- In a single pipeline



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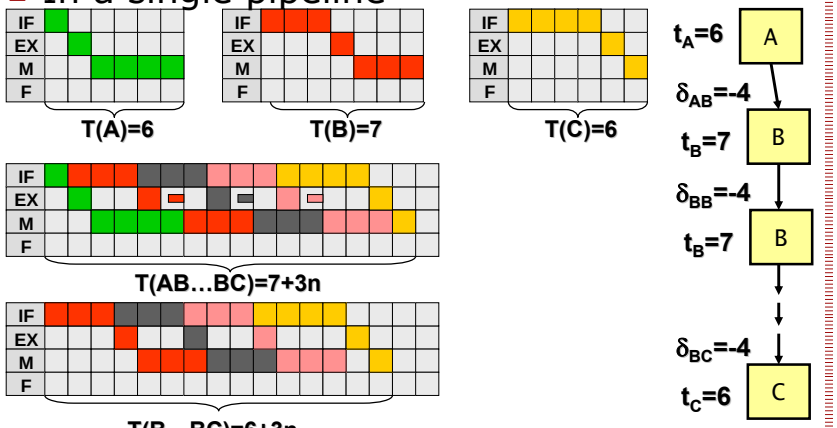
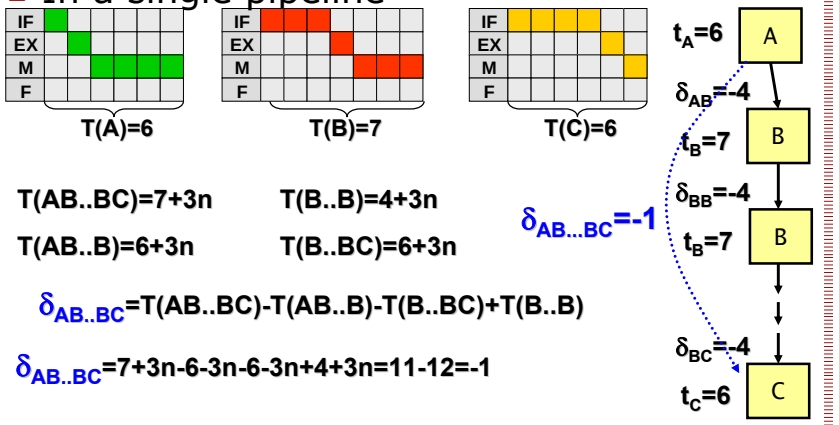
Unbounded LTE

- In a single pipeline



Unbounded LTE

- In a single pipeline



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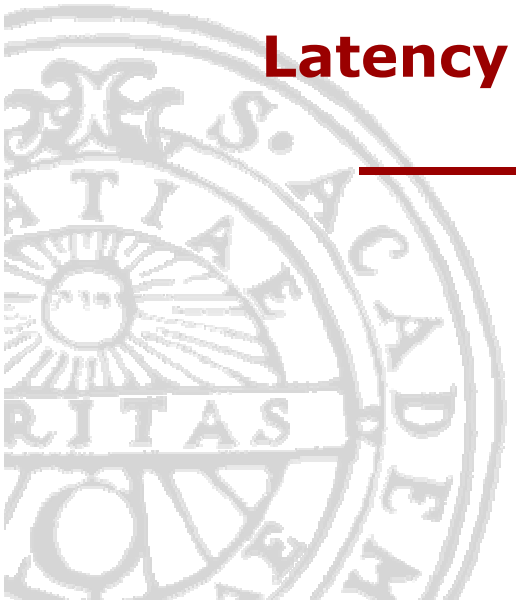
Unbounded LTE

- Not just negative
  - Example of positive effect in thesis
- Can appear in the simplest of pipelines (unexpected)
- Consequences:
  - Not obvious that analyzing up to some fixed maximal distance is safe
  - Analysis can get very complex



Latency Variations and LTEs

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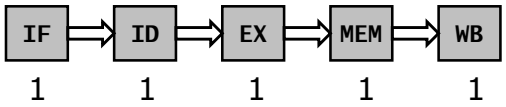
Results on LTEs

- Variable latencies ⇔ LTEs
  - No variable latencies in pipeline means no possibility of long timing effects
- Length of LTEs related to latencies
  - Highly irregular patterns
- Some examples for a 5-stage pipe
  - Simulation study
  - Assuming no data dependences

Example



Perfect pipeline, no LTEs

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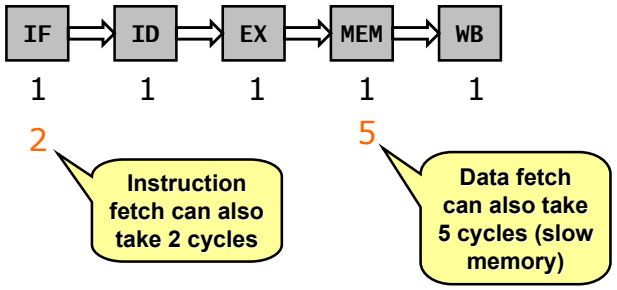
Example



LTEs up to length 4 occurs

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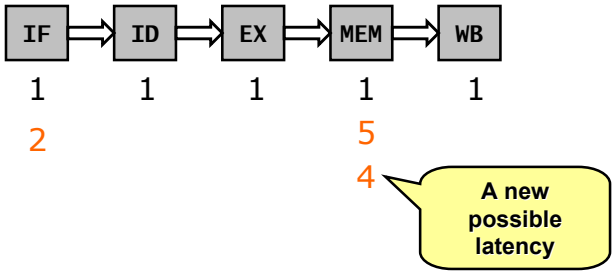
Example



LTEs still on length 4 max

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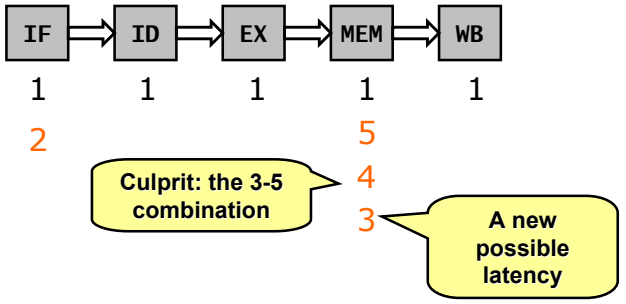
Example



Suddenly, LTEs of length 6

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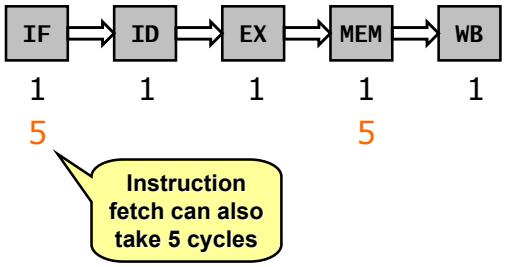
Example



LTEs of infinite length occur